Cryogenic Thermal Management of Power Conversion Devices on Liquid Hydrogen Fueled Electric Aircraft

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Abstract. Cold plate designs for cryogenic power conversion systems were studied using finite element method in COMSOL as part of the thermal management strategy for a superconducting power system of a liquid hydrogen-fueled electric aircraft. The 20 K liquid hydrogen also serves as a cryogenic heat sink for thermal management. The models were first developed for water-cooled room-temperature systems to validate them by comparing the results with those published in the literature. The validated models were utilized to investigate the cryogenic thermal management of cryogenic power conversion systems. Closed-loop cryogenic helium gas circulation was used as the cooling mechanism. The use of cryogenic helium significantly improved heat transfer and lowered system temperature, resulting in reduced thermal resistance. The cold plate design used for cooling power electronic circuits helps mitigate localized hotspots. The future work that was suggested includes developing cryogenic thermal models for multichip converter systems. Coolant flow path design optimization and temperature regulation were proposed to achieve a target device junction temperature of 120 K.

1. Introduction

Cryogenic power conversion systems are being developed to support liquid hydrogen (LH2) fueled electric aircraft with superconducting power devices. The benefits and the need for operating power conversion systems at cryogenic temperatures to increase system-level efficiency and lower the complexity of transition interfaces between room-temperature and cryogenic power system components have been reported [1]. Detailed cryogenic thermal characterization of power conversion systems is crucial for designing and developing the necessary cooling methods for these systems.

There is a need for multiple power conversion devices in the power system of an electric aircraft. The multimegawatt power system components and power conversion systems will create significant thermal loads. Thermal management of superconducting power systems presents a challenge because these systems must operate within narrow bands of cryogenic temperatures. The transition of power from room-temperature components to cryogenic superconducting systems through current loads produces significant heat due to the expected ampacities of several kA. Operating power conversion systems at cryogenic temperatures reduces the heat loads because of the significantly reduced resistances of the components and the elimination of transitions from room temperature to cryogenic temperature interfaces.

The limited cooling budget available for LH2-fueled electric aircraft makes it essential to minimize the heat loads from all devices, including power conversion systems. Effective modeling and experimental validation of thermal loads and cryogenic cooling techniques are necessary for the successful design of cryogenic power conversion systems for electric aircraft.

Power electronic components generate significant heat due to energy losses during operation. These losses mainly stem from switching and conduction phenomena. Switching losses occur during transitions between conduction and blocking states, where substantial voltage differences exist across the device terminals [2]. The product of energy lost per switching event and the operating frequency quantifies switching losses. In contrast, conduction losses are tied to the device's duty cycle and happen when it is fully conducting.

1.1 Testbeds for Cryogenic Power Conversion Systems

Figure 1(a) illustrates a cryogenic power electronics characterization setup where the temperature is regulated by partially submerging power electronic test objects in liquid nitrogen [3]. This method features a simple design and control strategy, offering low-cost implementation. However, the setup is not airtight, making it incapable of controlling internal air pressure. Figure 1(b) depicts a more advanced testbed, where the power device is directly cooled using liquid nitrogen [4]. Gaseous nitrogen acts as an insulating layer to prevent condensation and freeze water vapor from ambient air. The cryogenic chamber is well-sealed and safe, effectively avoiding leaks and preventing injuries caused by high pressure or extreme cold. It also provides excellent thermal insulation, safeguarding operators from cryogenic hazards. Furthermore, the gas insulation minimizes moisture freeze-up, thereby reducing the risk of short circuits.

The proposed approach in this work aims to eliminate the added complexity, cost, weight, and volume associated with using separate cooling systems. In the presented design, power electronic components are mounted on the drilled side of a cold plate. A Thermal Interface Material (TIM) is applied to enhance thermal conductivity while ensuring electrical insulation between the components and the cold plate. Heat is removed through a cooling mechanism where coolant flows through internal channels within the cold plate.

During the past few decades, the heat flux density from electronic components has increased dramatically, from approximately 0.5 W/cm^2 in the 1980s to 40 W/cm^2 in the 2000s, with projections exceeding 250 W/cm^2 in recent years [5]. These levels approach those seen in extreme environments like nuclear reactors and space re-entry vehicles, posing serious reliability risks. Standard ICs today can dissipate up to 100 W/cm^2, while advanced Very Large-Scale Integration (VLSI) systems can reach 10^3–10^4 W/cm^2.

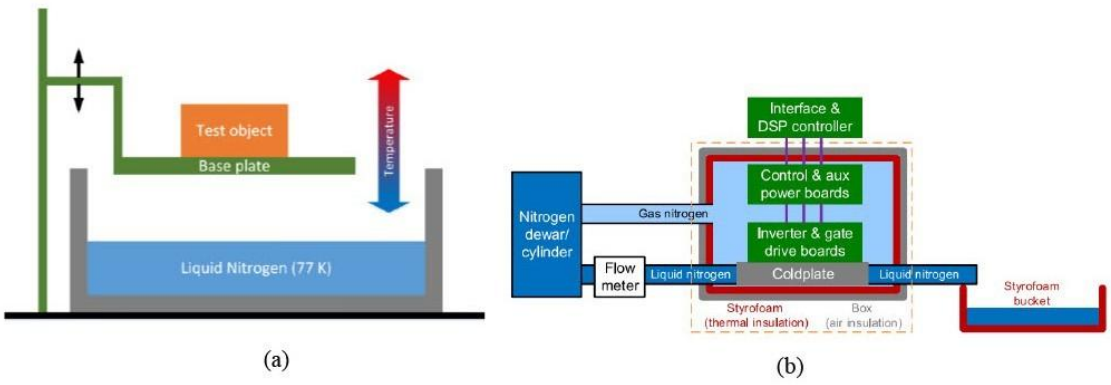

Figure 1. Cooling Cryogenic Power Conversion Systems [3,4].

High heat flux leads to rapid increases in temperature at the chip level, negatively affect performance, reliability, and life span [6]. Nonuniform temperature distributions further exacerbate the risk of localized failures. In addition, power electronic modules often operate under high current densities and steep thermal gradients. Their low thermal mass makes them particularly vulnerable to thermal runaway, which can occur in millisecond time scales.

Thermal management is further complicated by the multiple layers of material in the module packaging. These layers create thermal resistances between the chip and the cooling system. The overall heat removal capability is limited by the cumulative thermal resistance of each layer. In addition, thermal cycling causes mechanical stress due to mismatches in coefficient of thermal expansion (CTE) between adjacent materials, which risks long-term structural failure [7]. Maintaining junction temperatures below critical thresholds (typically 125 °C to 175 °C for silicon power chips) is essential to avoid issues such as short circuits. Thus, efficient cooling systems are vital to ensure the durability and performance of components.

Thermal management approaches fall into two categories [8]: 1) Passive Cooling: Using heat sinks and spreaders that rely on conduction and natural convection. 2) Active cooling: Enhances heat removal using electrically driven systems like forced air or liquid cooling. For moderate heat levels (50 W/cm^2), forced air cooling with finned elements is sufficient [9]. However, space constraints in integrated designs often require the use of heat pipes to transport heat to remote sinks [9].

Baseplate cold plates can handle up to 100 W/cm^2; Integrated cold plates (without thermal grease interfaces) are suitable up to150 W/cm^2. Microchannel heat exchangers and water jet impingement systems provide cooling up to 250 W/cm^2. Phase-change cooling technologies can support fluxes up to 1000 W/cm^2 [10].

Effective thermal design not only maintains safe operating temperatures but also enhances module performance, allowing for increased output currents and high-power densities using the same silicon area. Hadad et al. [11] conducted a numerical study on the influence of varying channel distribution and flow rate in straight mini-channel copper cold plates to mitigate on-chip hotspots [11]. Paper reported that directing a greater portion of the coolant flow toward the hotspot—and further increasing the concentration of flow in that region—enhanced the thermal performance of the cold plate, albeit at the cost of increased pump power.

Modifications of the mini-channel cold plate, along with combinations of different cooling strategies, have been explored in the literature [5]. However, notable differences exist in how these cooling methods are evaluated across studies [10]. The differences include variations in chip power distribution (uniform vs. nonuniform), cold plate and coolant materials, performance assessment metrics, and coolant inlet conditions. A direct comparison of cold plate performance using room-temperature water-cooled and cryogenic helium gas while keeping other factors, such as chip power map, materials, and inlet conditions constant, has not been comprehensively addressed.

The Integrated Zero Emission Aviation (IZEA), a NASA-funded University Leadership Initiative (ULI) program, is developing the liquid hydrogen (LH2) fueled electric aircraft concept. The IZEA's cryogenic thermal management strategy involves the use of LH2 as a heat sink, and secondary loops with supercritical helium gas will transfer the heat from power devices to the heat sink. As part of our thermal management studies, we are exploring cryogenic power conversion systems and developing effective cooling methods for them. Detailed cryogenic thermal models are crucial for developing effective cooling strategies. This paper describes the development of finite element analysis thermal models using COMSOL software. As an initial

design, we used mini-channel cold plate designs for room-temperature power electronic circuits. Key performance indicators such as chip-level temperature distribution, temperature non-uniformity, and thermal resistances are evaluated. The cold plate design is suitable for additive manufacturing techniques.

2. Model validation using room temperature model

The cold plate model was validated based on the study of Ansari and Kim [5]. Figure 2(a) presents the schematic of one-quarter of the base cold plate design featuring straight microchannel, while Figure 2(b) illustrates a side view of a half-model. The cold plate receives coolant through a single inlet port and discharges it through a single outlet port. A 0.1 mm thick TIM is positioned between the cold plate and the chip, which is mounted at the bottom of the cold plate. The schematic of the square chip is displayed in Figure 3. A square hotspot is located at the center of the chip. Table 1 provides the common model dimensions for cold plate configurations analysed in this study.

The given heat flux values for the hotspot and the background are 150 W/cm^2 and 20 W/cm^2, respectively. Although the hotspot occupies only 16 percent of the chip area, its heat flux is 7.5 times higher than that of the background. The total chip power is 255 W as assigned in [5]. The channel length (l_C) is 25 mm. The oblique manifold wall at the channel inlet and outlet (l_M) measures 10 mm and is angled at 30 degrees. The ten straight minichannels shown in Figure 2(a) each have 1 mm thick walls (t_{CW}) and a channel width (w_C) of 1 mm. The height (h_C) of both channels and channel walls is 6 mm, and the external length of the inlet/outlet ports (l_{IO}) is 3 mm. The coolant inlet temperature (T_{in}) is maintained at 293.15 K. The study considers four volumetric coolant inlet flow rates (qv): 2.84, 3.55, 4.26, and 4.97 cm^3/s.

The coolant flowing through the cold plate's channel removes heat generated by power electronics components. Liquid cooling can potentially yield high heat transfer coefficients due to the favourable thermophysical properties of liquids, especially when combined with narrow flow

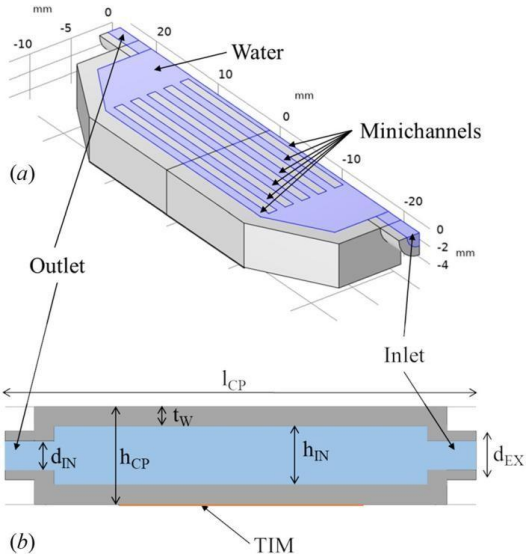

Figure 2. (a) Schematic of a quarter of base cold plate model with straight microchannels and (b) side view of a half model. A thin layer of TIM separates the cold plate from the chip [5].

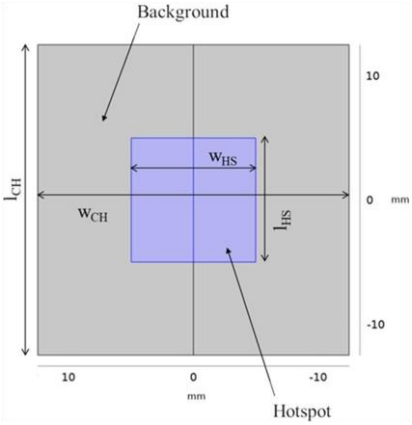

Figure 3. A 10 mm × 10 mm hotspot is located at the center of a 25 mm × 25 mm chip [5].

Table 1. Common dimensions for all cold plate configuration.

Definition	Symbol	Value (mm)
Wall thickness	t_W	2.0
Inlet/outlet ext. dia.	d_{EX}	5.0
Inlet/outlet int. dia.	d_{IN}	3.0
TIM thickness	t_{TIM}	0.1
Overall cold plate height	h_{CP}	10
Cold plate Internal height	h_{IN}	6.0
Cold plate total length	l_{CP}	48
Cold plate width	w_{CP}	25
Chip width	w_{CH}	25
Chip length	l_{CH}	25
Hotspot width	w_{HS}	10
Hotspot length	l_{HS}	10

paths that provide an increased surface area for heat exchange [11]. This study explores the feasibility of comparing temperature profiles cooled by room- temperature water and cryogenic helium gas, circulating within a cold plate, to extract heat from power electronic components.

The rationale behind adopting cryogenic cooling for power electronics stems from several factors. In systems such as electric aircraft, where cryogenic fluids are already present, integrating power electronics into the existing cryogenic cooling infrastructure can be advantageous. Without such integration, additional components like thermally insulated enclosures would be necessary to maintain required temperatures, thereby increasing system complexity, size, cost, and weight. Cryogenic cooling also offers notable performance benefits: enhanced efficiency of power semiconductor devices like Si and GaN due faster speeds and lower on-state resistance; decreased weight and volume of passive components at low temperatures; lower cooling demands due to reduced ambient temperature; and improved conductivity of materials like copper and aluminium, leading to lighter and more efficient bus bars and inductor windings [12].

2.1 Boundary Conditions

Figure 4 illustrates the boundary conditions used for the numerical simulation of the cold plate configuration shown in Figure 2 [5]. Due to the symmetric geometry and thermal loading of the model, a symmetry boundary condition on its center line was applied to reduce computational effort. In Figure 4(a), the coolant enters the cold plate through the inlet velocity surface and exits via the outlet at constant pressure. The four inlet velocities mentioned earlier are specified as normal velocities. Constant heat fluxes, as previously described, are applied to both the hotspot and the background regions.

All external surfaces of the cold plate, except for the symmetry plane, are assumed to be adiabatic, i.e, surfaces of the cold plate (top, bottom, sides, etc.) are modeled as insulated — no heat leaks from the surroundings. The symmetry plane, indicated by the red dashed region, is assigned zero-gradient boundary conditions. As shown in Figure 4(b), all internal walls of the cold plate, excluding the symmetry plane, are subjected to no-slip boundary conditions.

2.2 Components of Cryogenic Power Conversion Systems

In cryogenic power conversion systems, component selection is crucial for ensuring performance and reliability under extreme low-temperature conditions. Semiconductor devices such as Si MOSFETs, GaN HEMTs, and Si IGBTs can be adopted in cryogenic applications that

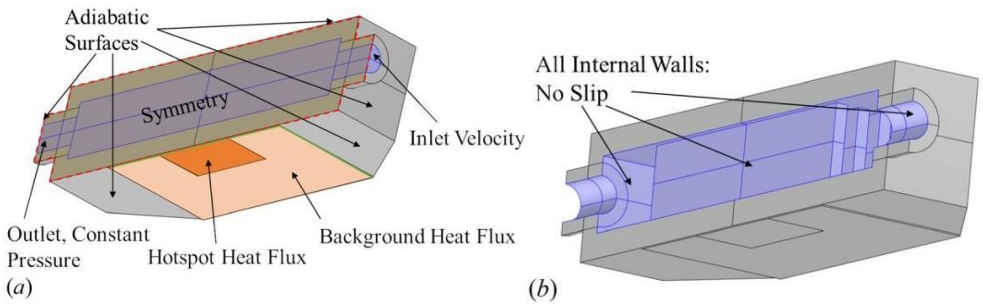

Figure 4. Schematics of (a) thermal and (b) fluid boundary conditions. Half-symmetry analysis was possible due to the symmetric geometry and boundary conditions [5].

require lower power loss. While SiC MOSFETs exhibit relatively poor conduction performance, they are more suitable for scenarios that demand high breakdown voltage [12].

For magnetic components, nano-crystalline materials are the better choice for inductors and transformers operating at cryogenic temperatures. Similarly, polypropylene is the preferred material for capacitors in such environments due to its favorable dielectric characteristics under cold conditions. When it comes to resistors, thin films, metal films, and wirewound types are considered the best options for cryogenic temperatures because of their stable resistance and reliability.

Solder materials must also be carefully chosen. PbSn alloy can operate effectively at cryogenic temperatures and maintains its ductility when it has a high lead (Pb) content. Indium or indium-based alloys offer considerably better performance in cryogenic conditions but are more expensive, which may limit their use in cost-sensitive applications.

Printed circuit boards (PCBs) typically possess sufficient mechanical strength for cryogenic use, and their dielectric performance is enhanced, exhibiting higher flashover breakdown voltage [13]. Additionally, most dielectric papers show improved dielectric characteristics at cryogenic temperatures, making them suitable for insulation and support within such systems.

3. Numerical Analysis

3.1 Basic Assumptions

The following assumptions were applied in the analysis conducted for this study: (1) the fluid flow is steady, three-dimensional, and incompressible; (2) laminar flow occurs within the channels; (3) gravitational effects are ignored; (4) heat generation due to fluid viscosity is considered negligible; (5) radiative heat transfer is not included; (6) solid material properties are assumed constant; (7) coolant properties vary with temperature.

3.2 Governing Equations

The governing equations for three-dimensional conduction–convection heat transfer, based on the assumptions listed above, are outlined below [5,11]: The continuity equation is:

$$\nabla \cdot \left(\rho_f V\right) = 0 \tag{1}$$

whereρ_f denotes the fluid density and V is the velocity vector. The momentum equation is:

$$\mathrm{V} \cdot \nabla\left(\rho_f V\right) = -\nabla P + \nabla \cdot \left(\mu_f \nabla V\right) \tag{2}$$

where P is the pressure and μ_f is the fluid's dynamic viscosity. The energy equation for the fluid is:

$$\mathrm{V} \cdot \nabla\left(\rho_f C_P T_f\right) = \nabla \cdot \left(k_f \nabla T_f\right) \tag{3}$$

where C_P is the fluid's specific heat at constant pressure, k_f is the thermal conductivity, and T_f is the fluid temperature. The energy equation for the solid is:

$$\nabla \cdot (k_s \nabla T_s) = 0 \tag{4}$$

where k_s and T_s represent the thermal conductivity and temperature of the solid, respectively.

3.3 Material Properties

The numerical model comprises a solid domain—composed of the cold plate body and a thermal interface material (TIM) and a fluid domain representing the coolant. Copper is selected as the material for the cold plate, while thermal grease is used as the TIM. The thermophysical properties of copper and the TIM are listed in Table 2. As previously noted, a temperature-dependent material model is employed for coolants [5]. The density (ρ_f), specific heat capacity (Cp), thermal conductivity (k_f), and dynamic viscosity (μ_f) of liquid water within the temperature range (293.15 K < T < 390 K), as used in COMSOL,

$$\rho_f = -950.70406 + 18.92294T - 0.06037T^2 + 0.00006T^3 \tag{5}$$

$$C_P = 12010.1471 - 80.4073T + 0.3099T^2 - 5.3817 \times 10^{-4}T^3 + 3.6254 \times 10^{-7}T^4 \tag{6}$$

$$k_f = -0.8691 + 0.0089T - 1.5837 \times 10^{-5}T^2 + 7.9754 \times 10^{-9}T^3 \tag{7}$$

$$\mu_f = 1.3799 - 0.0212T + 1.3605 \times 10^{-4}T^2 - 4.6454 \times 10^{-7}T^3 + 8.9043 \times 10^{-10}T^4 - 9.0791 \times 10^{-13}T^5 + 3.8457 \times 10^{-16}T^6 \tag{8}$$

are defined as functions of temperature in Kelvin.

3.4 Thermal Resistance

The thermal behaviour of a cold plate is characterized by its thermal resistance, as defined by Hadad et al. [11]:

$$R^{th} = \frac{A_{CH}\left(T_{c,max} - T_{in}\right)}{q_{CH}} \tag{9}$$

where, $T_{c,max}$ and T_{in} represent the maximum chip temperature and the coolant inlet temperature, respectively, while A_{CH} denotes the chip area. A lower thermal resistance indicates a higher rate of heat transfer, which is favourable for effective thermal management in microelectronic systems.

4. Discussion of Results

4.1 Result of Single Chip Model at Room Temperature:

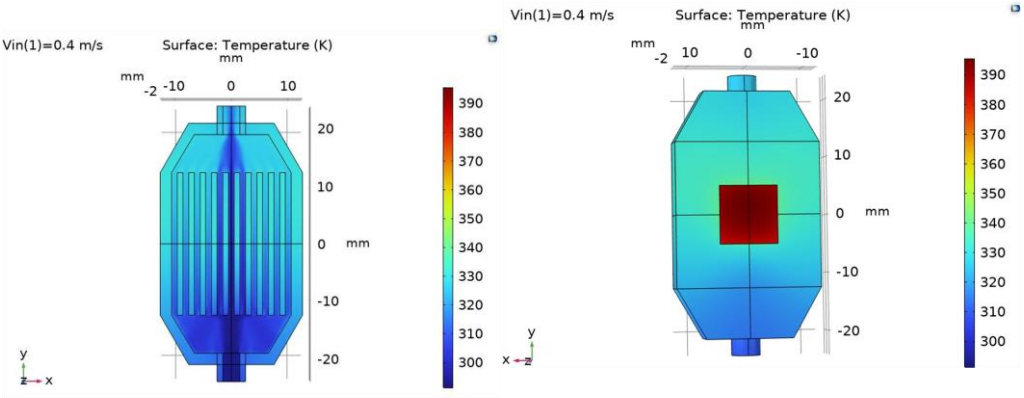

Figure 5. Models of Single Chip Results - Room Temperature.

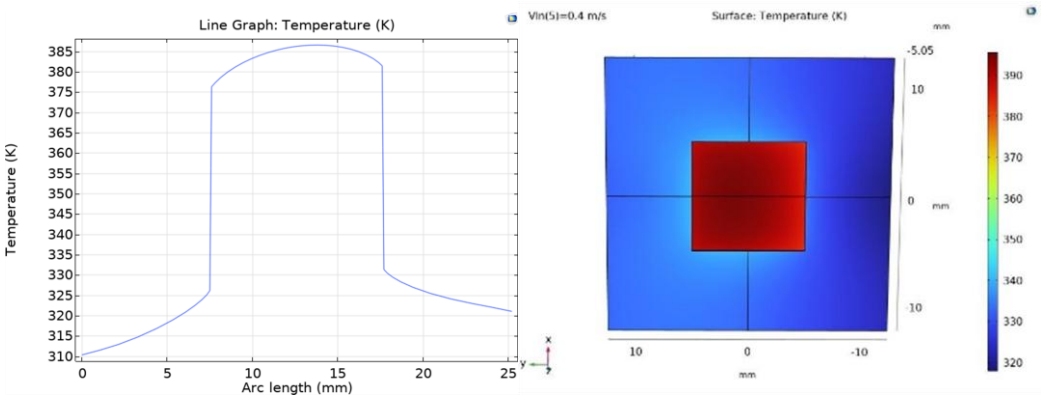

Figure 6. Chip temperature profile along the center line of the coolant flow and a chip-level temperature distribution for room temperature model

The model of single chip was simulated in COMSOL software shown in Figure 5 at the room temperature with water as a coolant. The inlet water temperature was set at 293 K. The different inlet velocities mentioned above are simulated, but the case with inlet velocity of 0.4 m/s is shown. From the Figure 5, the bottom half of the cold plate is displayed on the left and the full cold plate with the chip at the center is displayed on the right. The maximum temperature concentrated on the chip is about 390 K, which is well agreed with Ansari and Kim [5]. Figure 6 illustrates the chip-level temperature profile for simulated results along the coolant flow direction. The colour map in this figure visualizes the temperature distribution across the chip, revealing a notable temperature difference between hotspot regions and the surrounding areas, thereby confirming the presence of non-uniform temperature distribution.

4.2 Result of Single Chip Model at Cryogenic Temperature

The single chip model was simulated using COMSOL software under cryogenic conditions with gaseous helium as the coolant as seen in Figure 7. The flow and heat dissipation were simulated

Table 2. Thermophysical properties of copper and TIM.

	C_P(J/kg·K)	k(W/m K)	ρ(kg/m^3)
Copper	385	400	8960
TIM	1200	3	2600

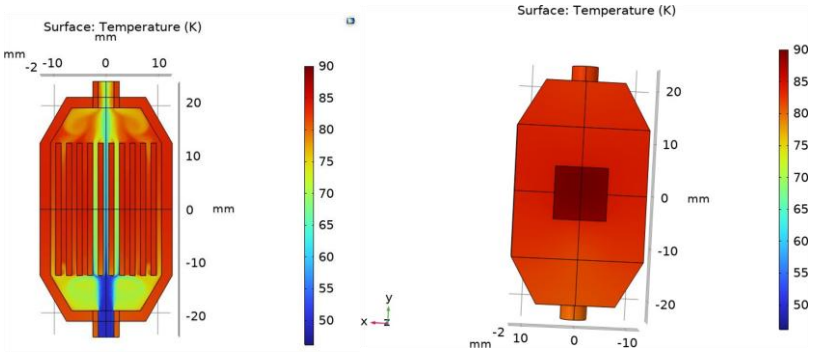

Figure 7. Chip temperature profile along the line of the coolant flow. A chip-level temperature distribution is shown.

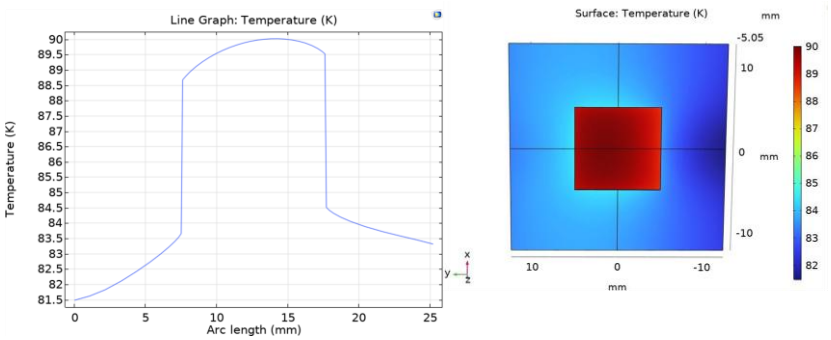

Figure 8. Chip temperature profile along the center line of the coolant flow and a chip-level temperature distribution for cryogenic model

using selected parameters. The three primary points of interest - the surface temperature of the power electronic component, the temperature at the farthest edge of the copper heat spreader, and the maximum temperature difference - were obtained. The coolant inlet temperature was set to 50 K, with a selected mass flow rate of 0.1 g/s and a pressure of 1.72 MPa (250 psi). In Figure 8, the left panel shows the temperature along the horizontal center line, while the right panel shows a full view of temperature distribution at the chip-level. It is observed that the maximum temperature reaches approximately 90 K, concentrated around the chip region near the center. The colour map illustrates the distribution of temperature across the chip, highlighting a clear temperature gradient between the hotspot and the surrounding areas. Compared to cooling at room temperature using water, cryogenic helium gas demonstrates significantly improved cooling performance, as evidenced by the results in Figures 7 and 8. The specific heat capacity of helium gas (C_P) is approximately 5 J/g K, and the temperature difference between the outlet and the inlet of $\Delta T = 75 - 50 = 25\ K$ was obtained. The heat removal can be expressed using the relation: $Q = \dot{m} C_P \Delta T \sim 0.1 \times 5 \times 25 = 12.5\ W$, which confirms the effective heat dissipation of preset chip's power dissipation of 12.5 W.

In the reported results, several simplifying assumptions were made, including idealized adiabatic boundaries, constant coolant properties across the temperature range, and constant outlet pressure. These assumptions allow the model to capture the overall cooling behavior and achieve good agreement with experimental studies, but they may neglect second-order effects such as heat leakage to the surroundings, and property variations of helium under cryogenic conditions. Accounting for these effects would improve model fidelity, though at the expense of higher computational complexity.

Future work will focus on extending this approach to larger-scale or more complex device geometries and a broader range of heat loads.

5. Conclusion

Finite element methods using COMSOL were employed to investigate the cold plate design of cryogenic power conversion systems as part of the thermal management strategy for a superconducting power system of an electric aircraft fueled by LH2, which also serves as a cryogenic heat sink at 20K. Cold plate designs were evaluated by developing water-cooled room-temperature systems and verifying the validity of the models through comparison with published literature. The validated models were utilized to investigate the cryogenic thermal management of cryogenic power conversion systems. Closed-loop cryogenic helium gas circulation was used as the cooling mechanism. The coolant type and the target operating temperature were the only variables that differed between the room temperature and cryogenic temperature analyses. The use of cryogenic helium significantly improved heat transfer and lowered system temperature, resulting in reduced thermal resistance. The cold plate design used for cooling power electronic circuits helps mitigate localized hotspots. It is essential to strike a balance between minimizing thermal resistance and ensuring a uniform temperature distribution across the chip. Future work will focus on developing cryogenic thermal models for multichip converter systems, including the design of coolant flow paths and temperature regulation strategies to achieve a target device junction temperature of 120 K.

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